System Level Modelling Environment for SMEs

(an ARTEMIS project)

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Outline

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- SYSMODEL project
- Modelling and simulation framework
- System modelling
- Platform modelling
- Design space exploration
- Interface and interoperation issues
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Motivation – system-level design

- System-level design increases design productivity and improves design quality
  - Better application specification
  - Easier design space exploration
  - Shorter prototyping phase
  - Possibility to use pre-defined hardware/software platforms (platform-based design)
Motivation – system design approach

• High-level model/specification mapped on HW (fixed, reconfigurable) and/or SW (plain, OS-based)
Motivation – modelling languages

- Several (HW/SW) system modelling languages exist, e.g.
  - SystemC
  - Java
  - UML (w/ specific profiles like MARTE)
  - Domain-specific languages
  - Tool-specific or vendor-specific languages/dialects
  - Graphical representations of systems
  - Other (exotic) languages
Motivation – open-source tooling

- Commercial system-level tools expensive for SMEs
- Open-source tools also more open for customization and inclusion of new (point) tools and models
- There exist several open-source tools for system modelling, e.g.
  - ForSyDe by KTH, Sweden
  - Ptolemy II by UC Berkeley, US
SYSMODEL project – overview

- ARTEMIS funding (national + EC)
- 11 partners from DK, SE, FI, NO
- Exclusively SMEs and universities
- Using open-source tools (+ some new point tools) for:
  - System modelling framework
  - Platform architecture framework
  - Design space exploration
SYSMODEL project – structure

WP7
Management
Project management, IPR management, dissemination

WP2
System models

WP3
Platform models

WP4
Design space exploration

WP5
Verification of models

WP6
Training

WP1
Framework

Awareness
Web, flyer, awareness seminar

SME target group
Core group: 7 SMEs in consortium
"Aware" SMEs (few hundreds)
"Unaware" SMEs (several thousands)
SYSMODEL project – approach taken

- Application requirements from SMEs
  - Time and power-critical heterogeneous embedded systems
  - Co-existence with current tooling in the companies
- Modelling capabilities from SW to AMS
- SystemC as language for models
- Creating a modelling framework mainly from existing tools
- Real applications and computation platforms as case studies
Modelling and simulation framework

- Basis for simulation, analysis and design space exploration
- Two major parts
  - System functionality framework (SFF)
  - Platform architecture framework (PAF)
- SFF built around KTH’s ForSyDe
  - Formal design framework extended to SystemC
- PAF based on a library of individual platform component models
System functionality framework

- ForSyDe supports
  - SystemC
  - VHDL (synthesizable subset)
  - C (algorithm level)
  - Matlab (high-level analog models)
- It also supports multiple models of computation (MoC)
Concurrent processes belonging to different models of computation communicate via domain interfaces.
System modelling

- SFF to support heterogeneous models of computation (MoC)
  - Untimed MoC
  - Synchronous MoC
  - Discrete-timed MoC
  - Continuous time MoC
- Modeling guidelines are being developed in the project
- Real applications of the SMEs as case studies
Platform modelling

- Model of the system architecture
- Consists of architecture components:
  - DSP, RISC, ASIC, FPGA, memory, interconnect (bus, NoC), peripherals
  - OS, SW components
- Different levels of models
  - High-level models of component properties for performance analysis
  - Transaction-level functional models (TLM) for simulation
  - Also RTL models can be cosimulated
C-algorithms and synthesizable VHDL can be co-simulated using SystemC wrappers!
Refinement by replacement

- An SFF process is replaced by a platform model
- SystemC wrappers allow simulation of refined models
Example platform – TUT Ninesilica

- Ninesilica is a 9-core instance of Silicon Café platform template
- Homogeneous instance of the platform
  - 9 similar open-source Coffee RISC Core (see http://coffee.tut.fi) clusters
  - Symmetric Mesh topology Network-on-Chip (NoC) interconnect
  - One core dedicated to control and I/O, eight cores run parallelized SW
- Runs on a single FPGA
Example platform – TUT Ninesilica

COFFEE CLUSTER

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I/O

EXTERNAL MEMORY
Example platform – TUT Ninesilica

• Component models in SystemC
  – Instruction-accurate Coffee instruction-set simulator in SystemC to run application code for functional simulation
  – TLM of the Network-on-Chip
  – Simple untimed memory models
  – (TLM of TCP/IP for system extension over ethernet connection)
Design space exploration

• Mapping from system models to platform models
• Analysis of the system realization characteristics
  • Performance
  • Cost
  • Effects of resource allocation and scheduling
• Point tool needed (to be developed)
Interface and interoperation issues

- Graphical user interface for the tools
  - Has to work in both Linux and Windows
  - Description-based QT considered (PAF)
- Eclipse explored as common platform for glueing tools together
  - Provides tooling to manage workspaces; to build, launch and debug applications
  - Could run tools as "plug-ins"
  - Might provide the GUI as well
  - Interoperation with Ptolemy II possible
Conclusions

- Open-source system-level modelling framework needed especially for SMEs
- SYSMODEL project is building such a framework as Nordic cooperation in ARTEMIS programme
- System functionality framework + platform architecture framework + design space exploration
- Work in progress, complete in 2011