Flash Memory Technology

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MCU Product Marketing Dept.2  MCU Product Marketing Div.
MCU Business Group
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Advantages of Using Microcomputers with Emb.-Flash Memory

- Reduced turn-around time (TAT) in development
  - Eliminating the masking process reduces TAT

- Reduced development and management costs
  - Elimination of mask ROM management costs
  - Reduced program-management costs

- Good for small quantities of multiple product variants

- Flash memory is reprogrammable in the field using the Internet or other means for convenient
  - Reprogramming of system code and parameters
Trend of Embedded Memory Capacity

Program memory size (MB) vs Year

- 1980: MASK 2~16kB
- 1990: OTP 64kB, MASK 32kB
- 2000: FLASH 256kB, FLASH 512kB
- 2010: FLASH 2MB, 4MB, 8MB

Automotive powertrain application

- 10 years x8

Program memory size (MB)

- 0.1
- 1
- 10

08/10/2008

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High Speed Flash Design

Small area penalty to achieve 100MHz

<table>
<thead>
<tr>
<th>Flash Module Size [A.U.]</th>
<th>Flash Read Speed [MHz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>0</td>
</tr>
<tr>
<td>1.0</td>
<td>50</td>
</tr>
<tr>
<td>1.5</td>
<td>100</td>
</tr>
<tr>
<td>2.0</td>
<td>150</td>
</tr>
<tr>
<td></td>
<td>200</td>
</tr>
</tbody>
</table>

NOR

MONOS
Why MONOS?

1. Excellent features of MONOS
   - No HV for word line (CG) and bit line (D)
   - No HV-transistor in read path
   - High speed read
   - Scalable across processes
   - Discrete charge storage
   - High Reliability

2. Long Experience with MONOS type NVM
   - Over 20 years of EEPROM & smartcard business
   - Over 2B pcs. of sales result
## High Speed Flash Design

<table>
<thead>
<tr>
<th>Design technology</th>
<th>Purpose (Effects)</th>
<th>NOR 0.5µ</th>
<th>NOR 0.35µ</th>
<th>NOR 0.18µ</th>
<th>MONOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal word line</td>
<td>Decrease word line resistance</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Divided bit line</td>
<td>Decrease bit line capacitance</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Differential sense amp.</td>
<td>High speed sensing</td>
<td>yes</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Boosted word line</td>
<td>Increase memory cell current</td>
<td>yes</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Two way word driver</td>
<td>High speed word driver (Refer ISSCC99/SESSION 6/PAPER MP6.8)</td>
<td>yes</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Int. down converter</td>
<td>Decrease Vdd fluctuation</td>
<td>yes</td>
<td></td>
<td></td>
<td>yes</td>
</tr>
<tr>
<td>Low voltage word driver</td>
<td>High speed word driver</td>
<td></td>
<td></td>
<td></td>
<td>yes</td>
</tr>
<tr>
<td>Hierarchical sense amp.</td>
<td>Decrease Bit line drive time</td>
<td></td>
<td></td>
<td></td>
<td>yes</td>
</tr>
</tbody>
</table>
• High speed design ~ Word line driver

- High voltage circuit
- Medium voltage circuit
- Low voltage circuit

**NOR**
- 0.5µm
- 20MHz
- Address decoder → Positive Level sifter → Negative Level sifter → High voltage WL driver → Word line

**NOR**
- 180nm
- 80MHz
- Address decoder → Positive Level sifter → Negative Level sifter → WL driver → Selector → Word line

**MONOS**
- 100MHz
- Address decoder → WL driver → Word line
Operating Frequency of MCU and Flash

Only Renesas achieves up to 100MHz single cycle access!
Summary

- CPU performance requirement is increasing and embedded flash performance is getting important.
- MONOS has strong feature of high speed, high reliability and process scalability. Renesas will use 65 and 45nm nodes.
- 100MHz single cycle access was achieved with small area penalty.
- First 90nm MONOS product shows excellent performance.
P/E Cycle Endurance of 0.2HND Flash (4KB)

Change in Program/Erase Cycle and Byte Program/Erase Time

P/E takes more time after P/E cycle reached 10K times. However, reliability and P/E characteristic do not present any problems.